

# EE 435

## Lecture 35

Dynamic Current Source Matching  
Charge Redistribution DACs  
ADC Design

# What Architectures are Actually Used

DACs  
Texas Instruments Mar 1, 2023

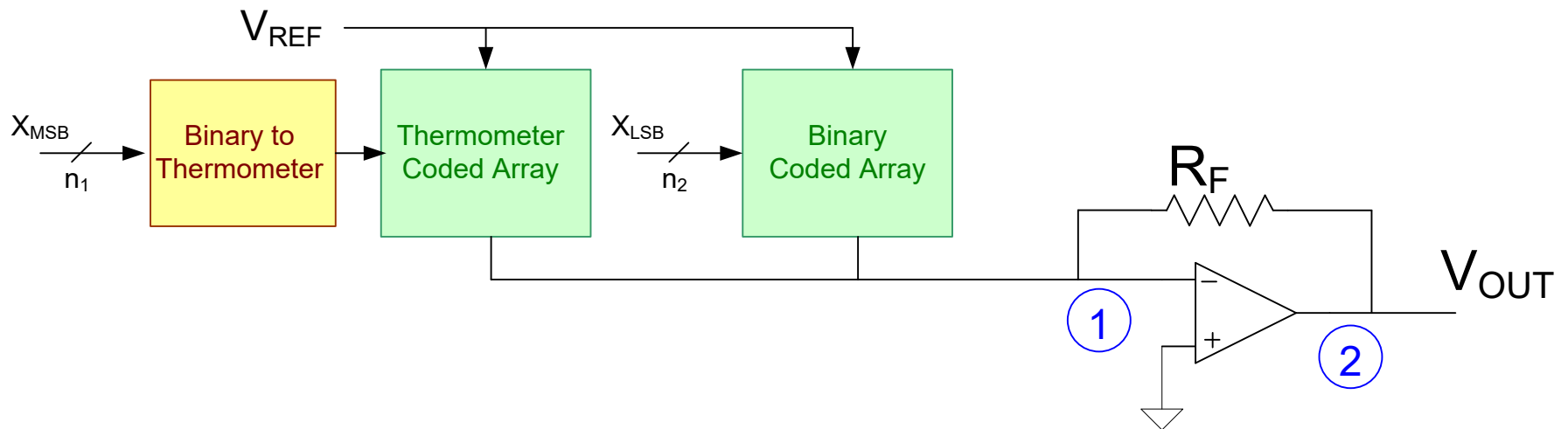
String	168
R-2R	79
Current Source	52
MDAC	23
Current Sink	17
SAR	9
Pipeline	7
Delta Sigma	4
1-Steering	3
Current Steering	2

ADCs  
Texas Instruments April 13 2023

SAR	728
Pipeline	294
Delta Sigma	187
Folding Interpolating	66
Delta Sigma	
Modulator	9
Two-Step	6
Flash	3
Total	1293

- These are catalog parts
- Specific details about architecture usually absent in data sheets
- Some (many) in list are slight variants and carry different part numbers
- Variety of converters used in ASIC applications will be larger

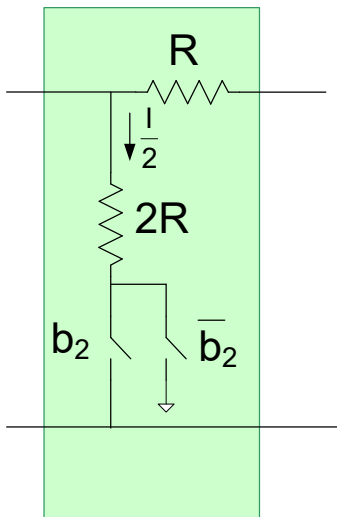
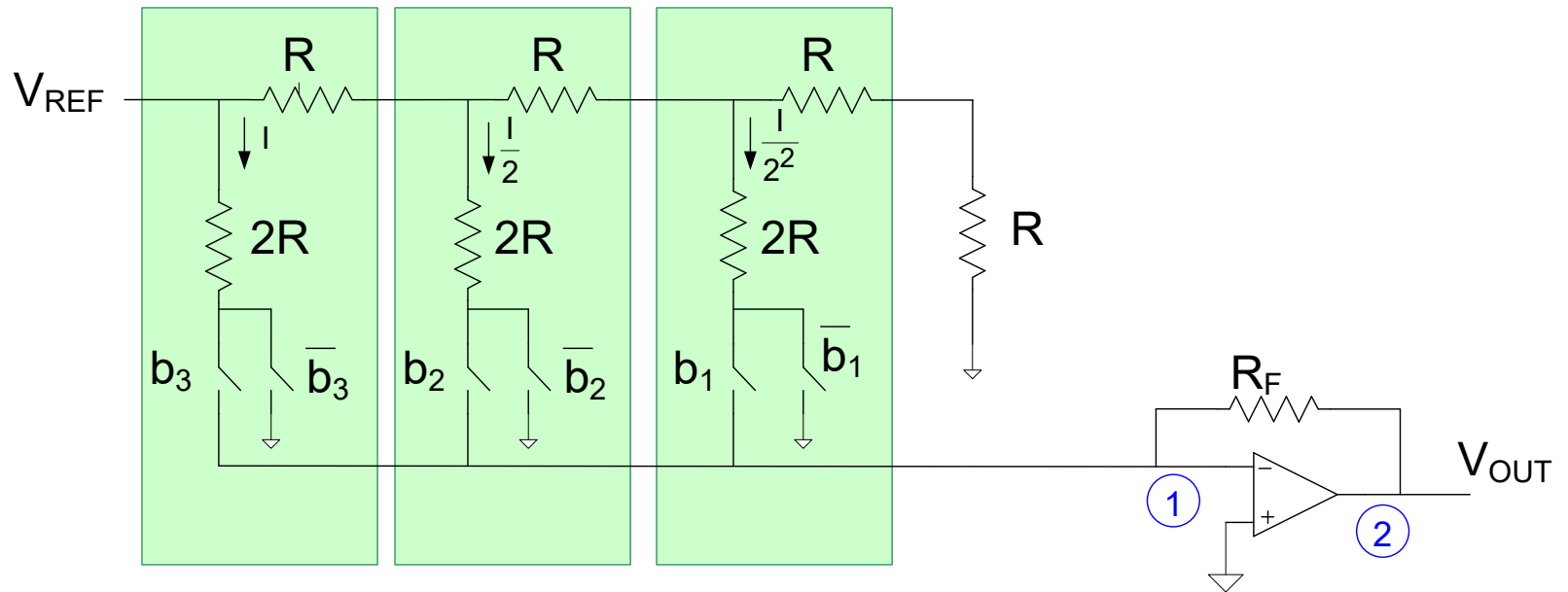
# Current Steering DACs



## Segmented Resistor Arrays

- Combines two types of architectures
- Inherits advantages of both thermometer and binary approach
- Minimizes limitations of both thermometer and binary approach

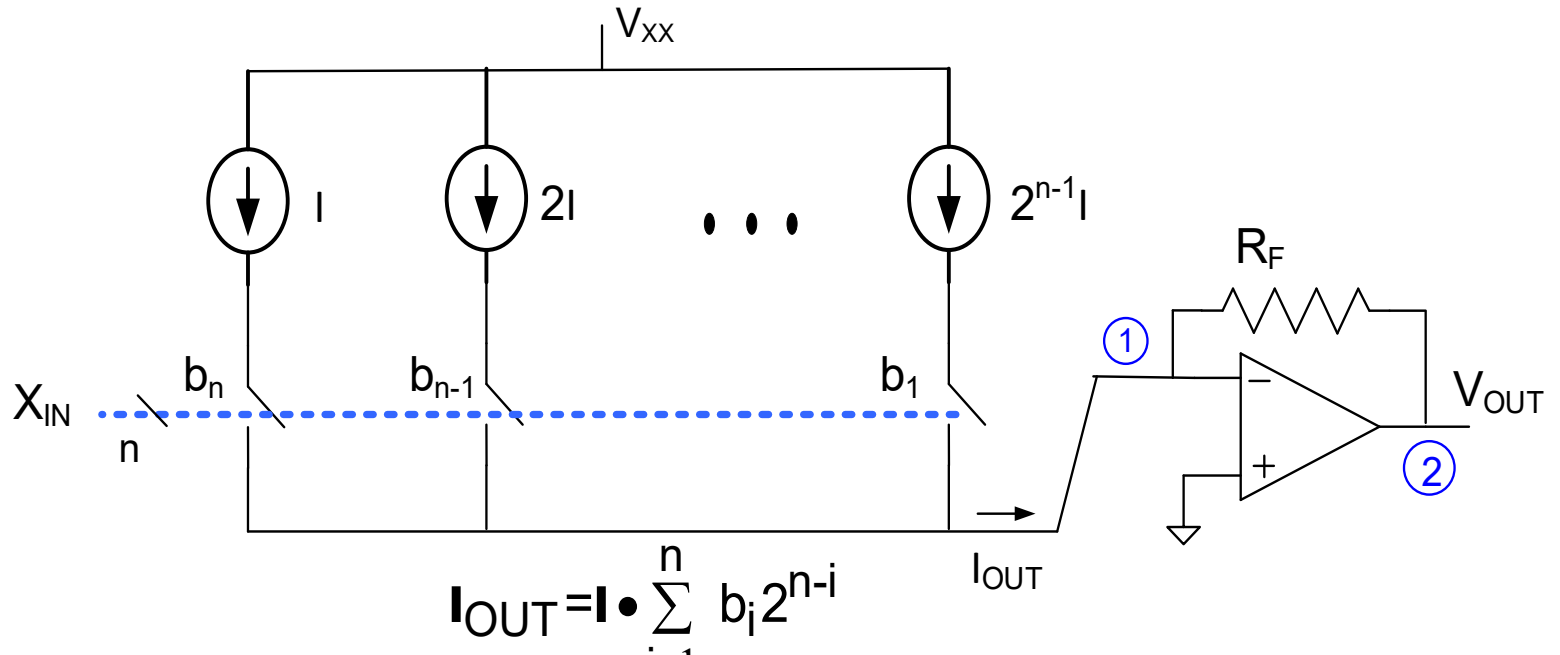
Review from Last Lecture  
Current Steering DACs



R-2R Resistor Arrays

Review from Last Lecture

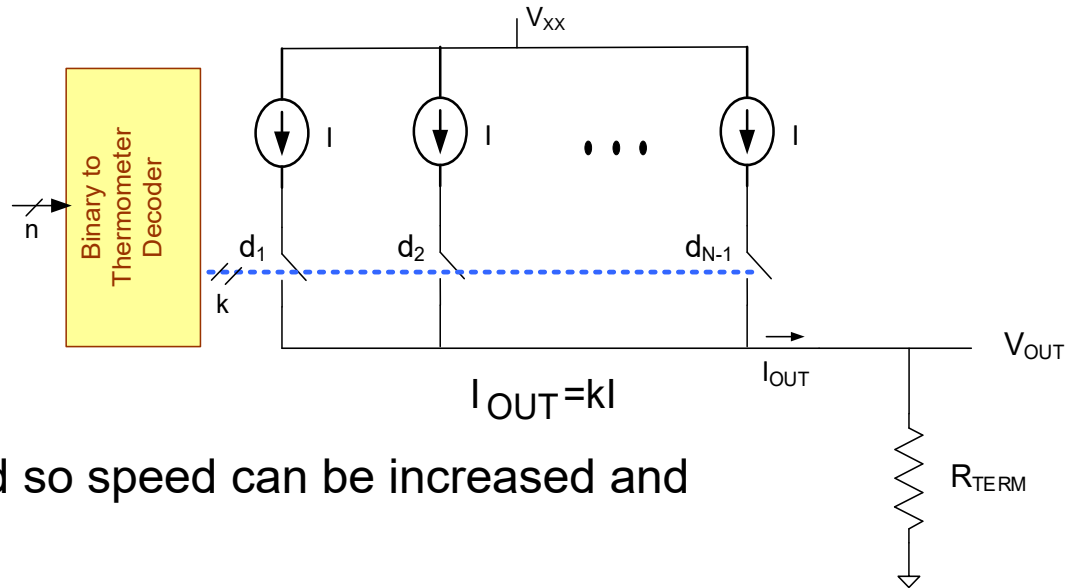
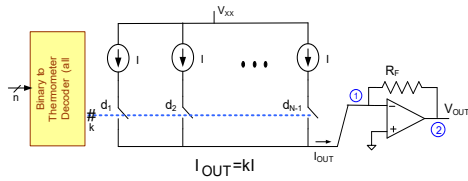
# Current Steering DAC



- Binary to thermometer decoder eliminated
- Current sources bundled unary cells
- Bundles large for large  $n$

# Review from Last Lecture

## Current Steering DAC



Op Amp can be eliminated so speed can be increased and power reduced

$R_{TERM}$  often 50 $\Omega$  or 100 $\Omega$

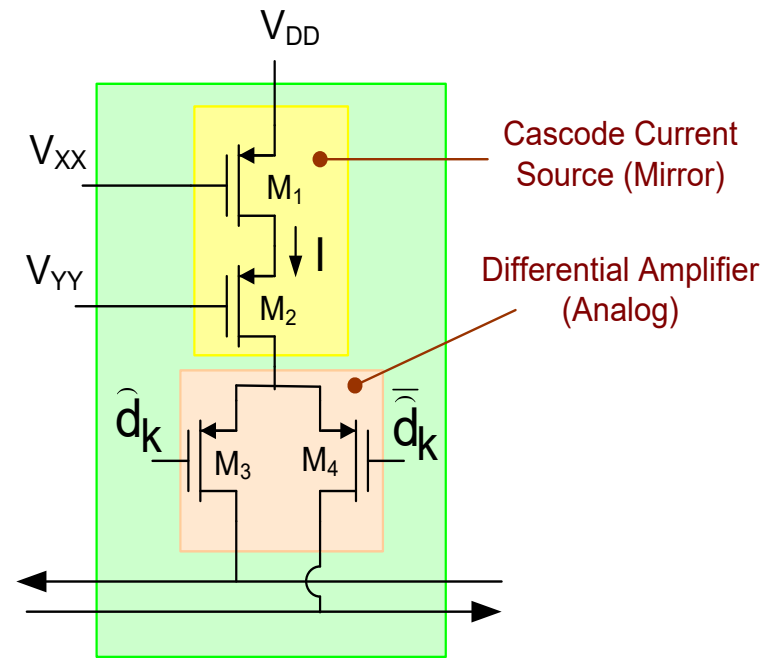
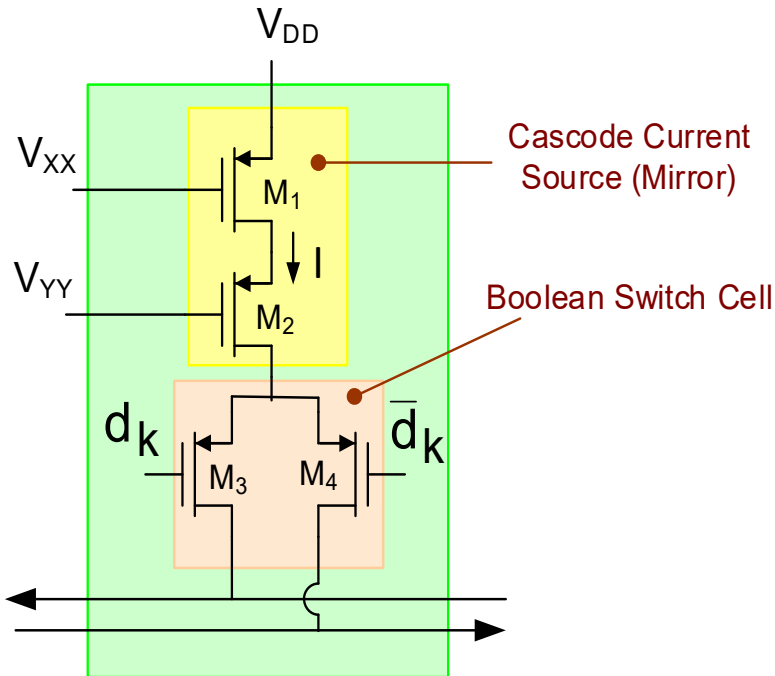
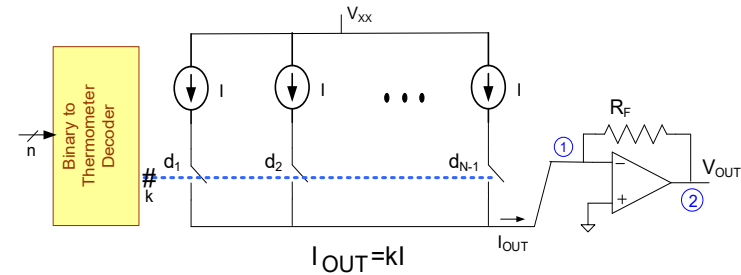
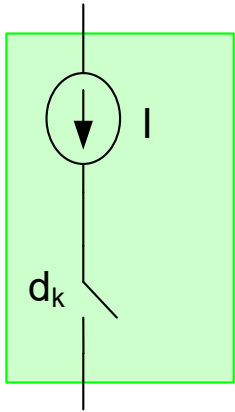
$R_{TERM}$  can be internal or external

Switch impedance now of concern

Output impedance of current sources now of concern

# Review from Last Lecture

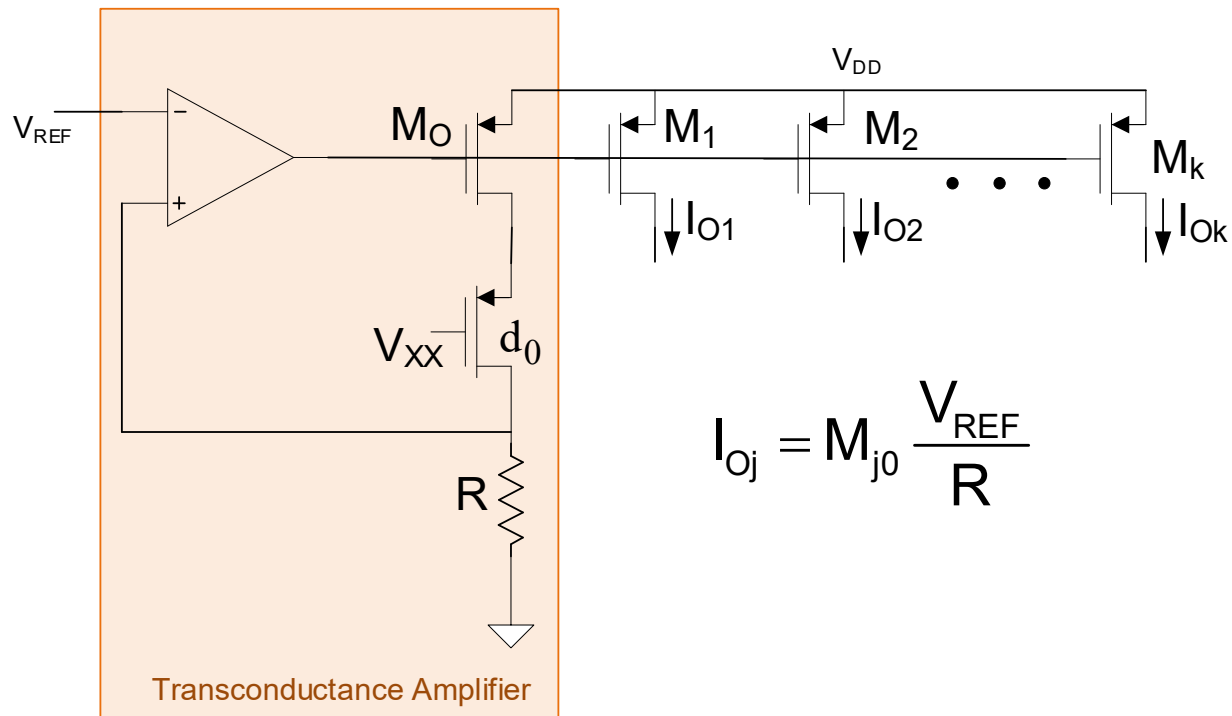
## Current Steering DAC



Steer rather than switch current  
Reduced swing on control signals

## Review from Last Lecture

# Multiple-output Transconductance Amplifier

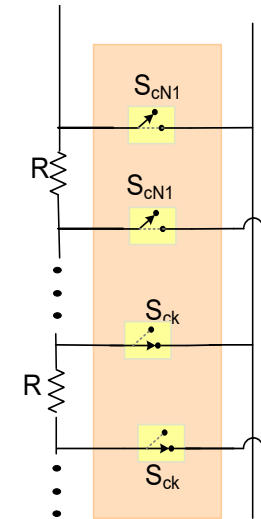
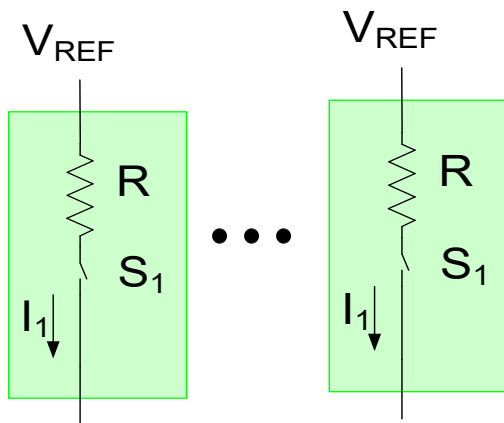
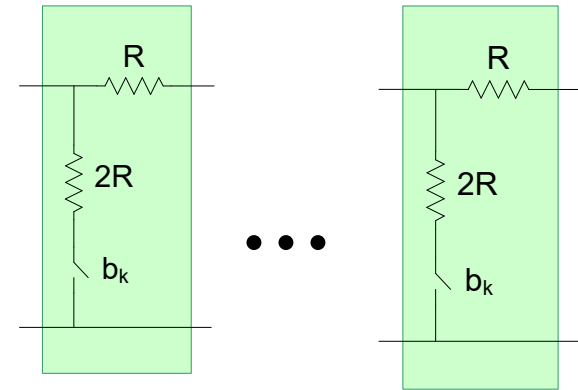
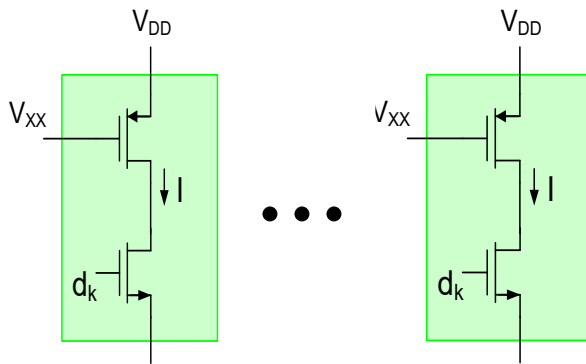


- Good linearity
- Each additional output requires only one additional transistor



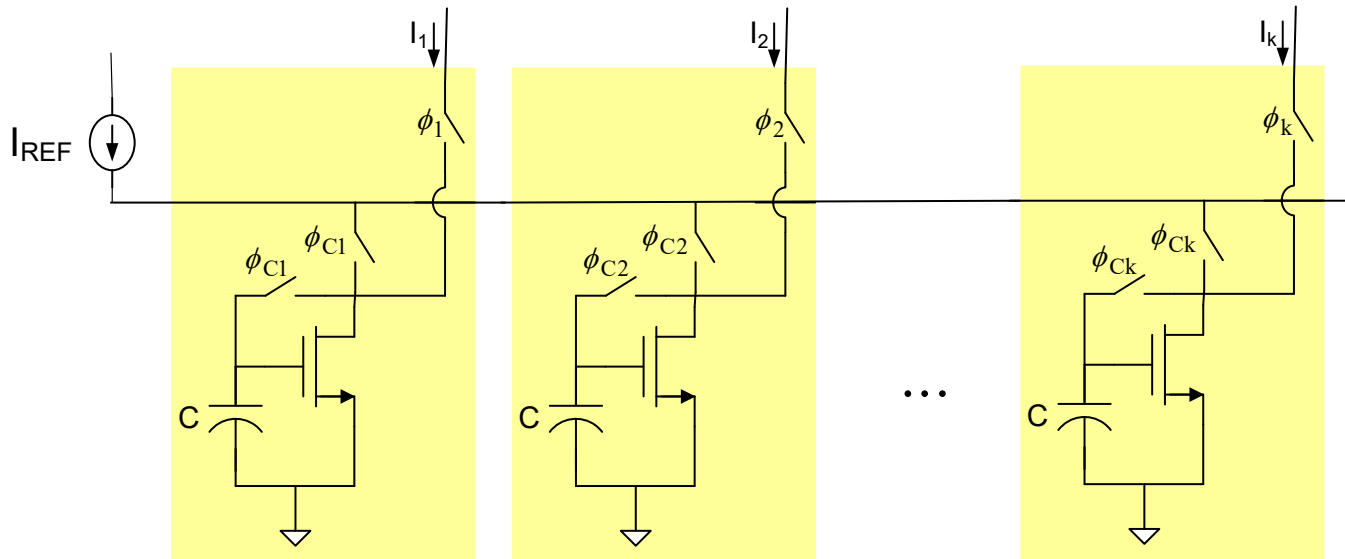


# Matching is Critical in all DAC Considered



Obtaining adequate matching remains one of the major challenges facing the designer!

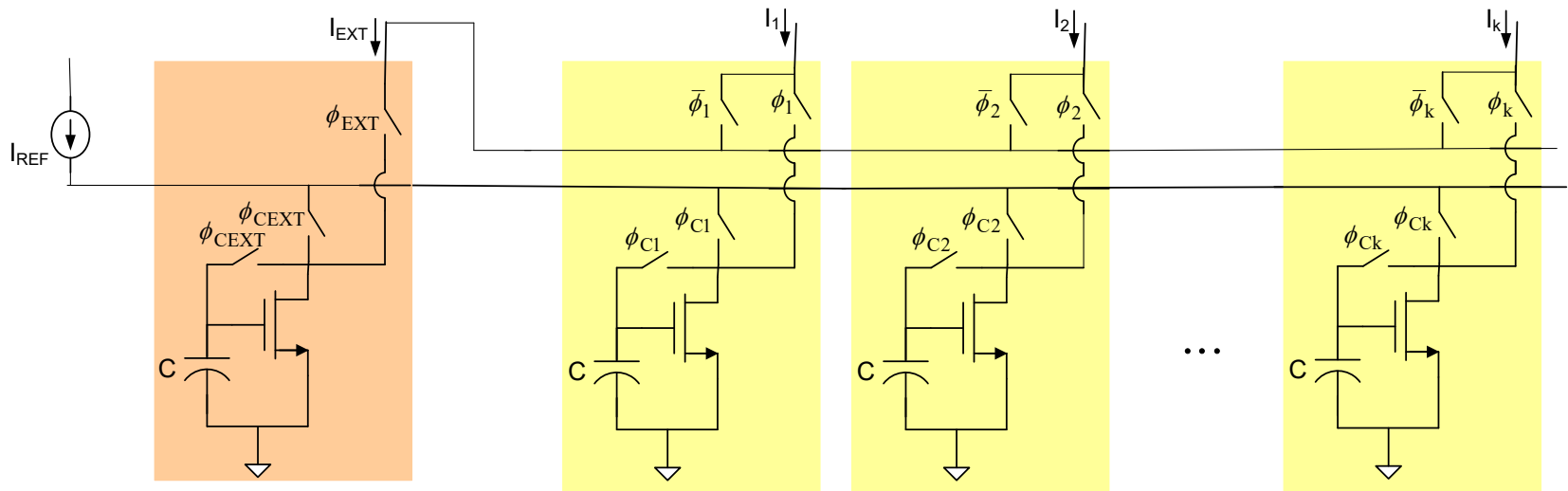
# Dynamic Current Source Matching



- $\phi_1, \dots, \phi_k, \dots, \phi_n$  distinct from  $d_1, \dots, d_n$  (not shown)
- Correct charge is stored on  $C$  to make all currents equal to  $I_{REF}$
- Does not require matching of transistors or capacitors
- Requires refreshing to keep charge on  $C$
- Form of self-calibration
- Calibrates current sources one at a time
- Current source unavailable for use while calibrating
- Can be directly used in DACs (thermometer or binary coded)

Often termed “Current Copier” or “Current Replication” circuit

# Dynamic Current Source Matching



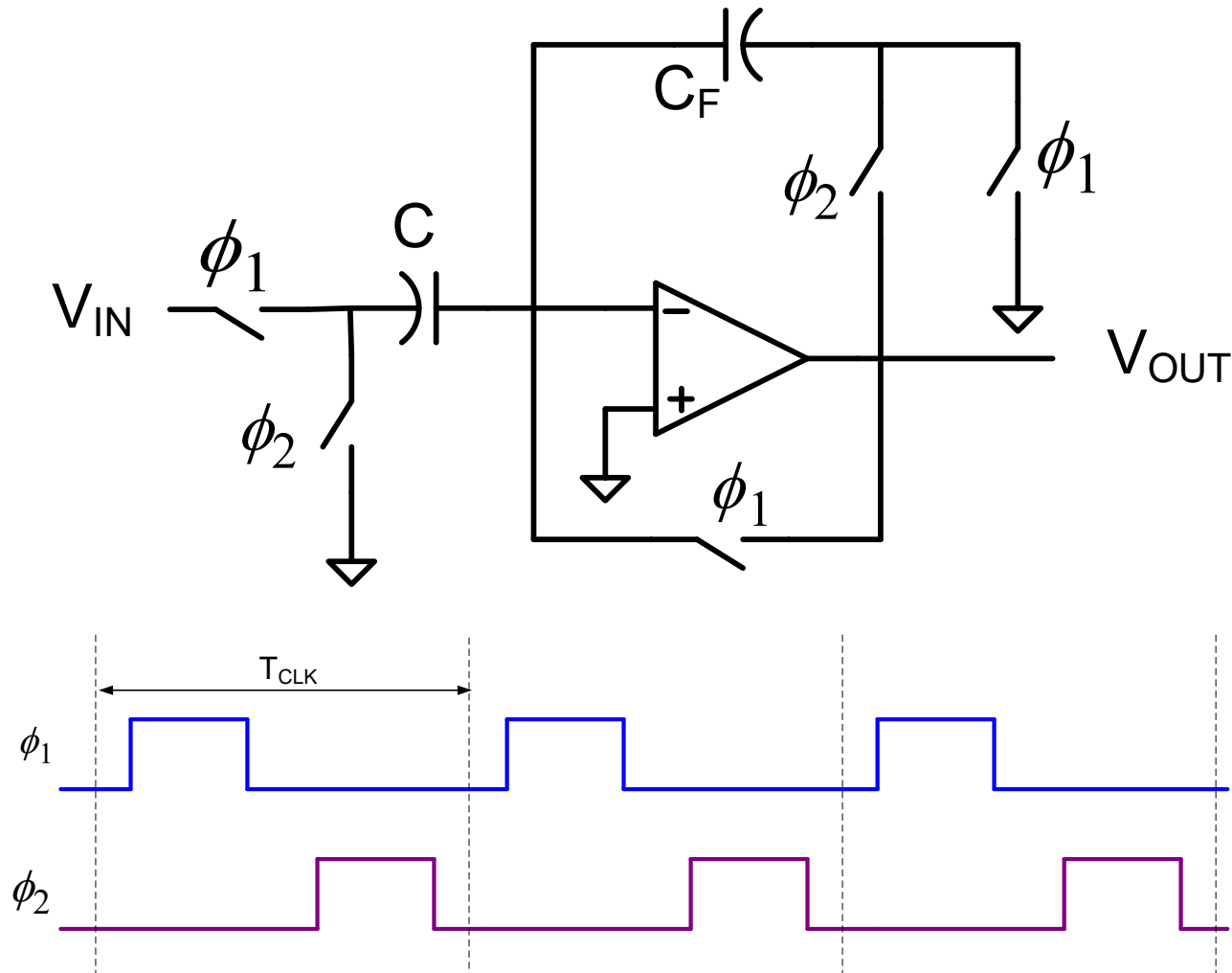
Extra current source can be added to facilitate background calibration

# Charge Redistribution DACs

- Previous DACs based upon matching of resistors or transistors
- Switch impedance was of concern in most of the structures
- Capacitor matching can be very good in most processes and area required for a given level of matching may be smaller for capacitors than for resistors or transistors in some processes
- Capacitor linearity is often excellent

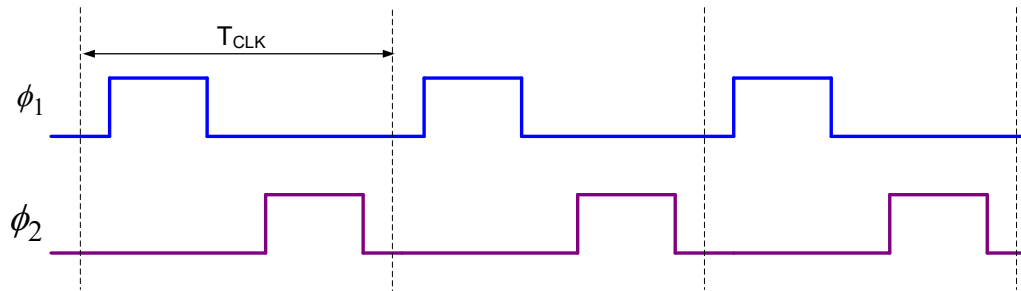
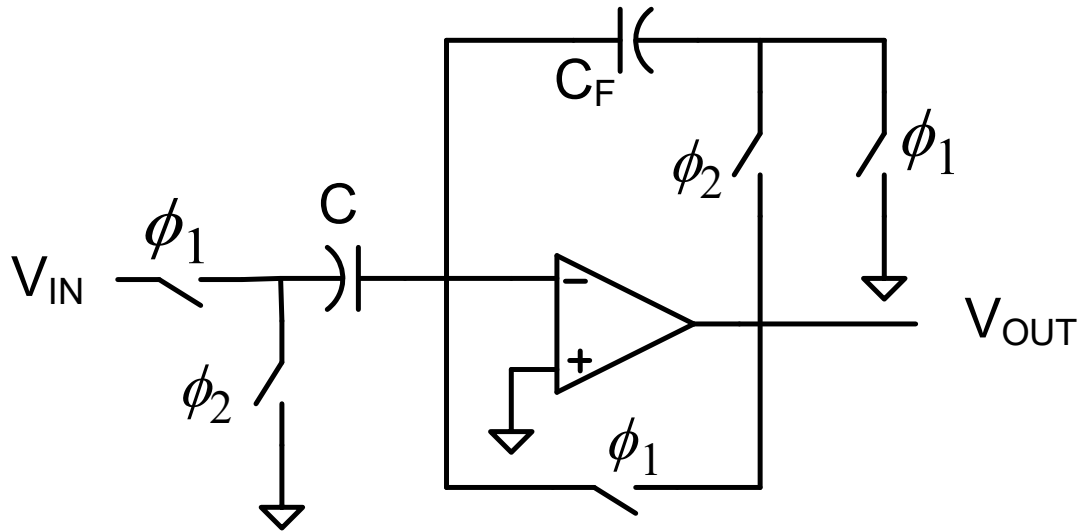
Will now focus on building DACs that take advantage of good capacitor matching and linearity

# A charge redistribution circuit



Clocks are complimentary non-overlapping

# A charge redistribution circuit



During phase  $\phi_1$

$$Q_{\phi_1} = CV_{IN}$$

$$Q_{CF} = 0$$

During phase  $\phi_2$

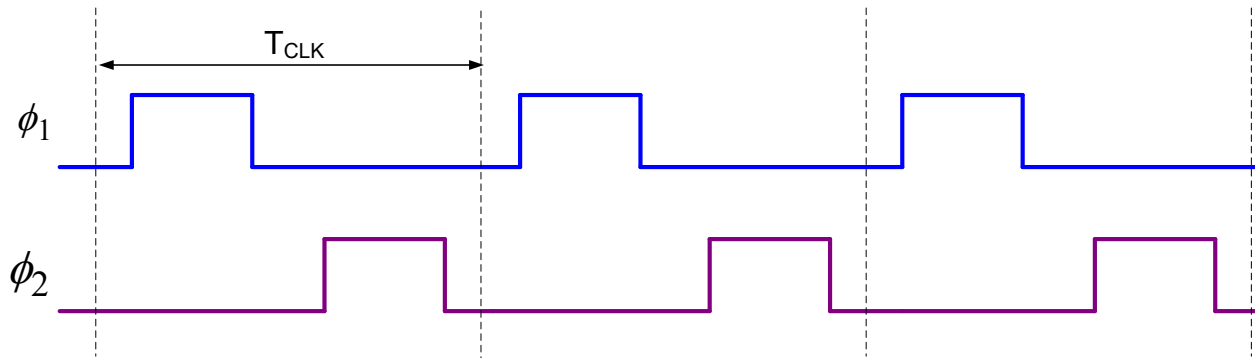
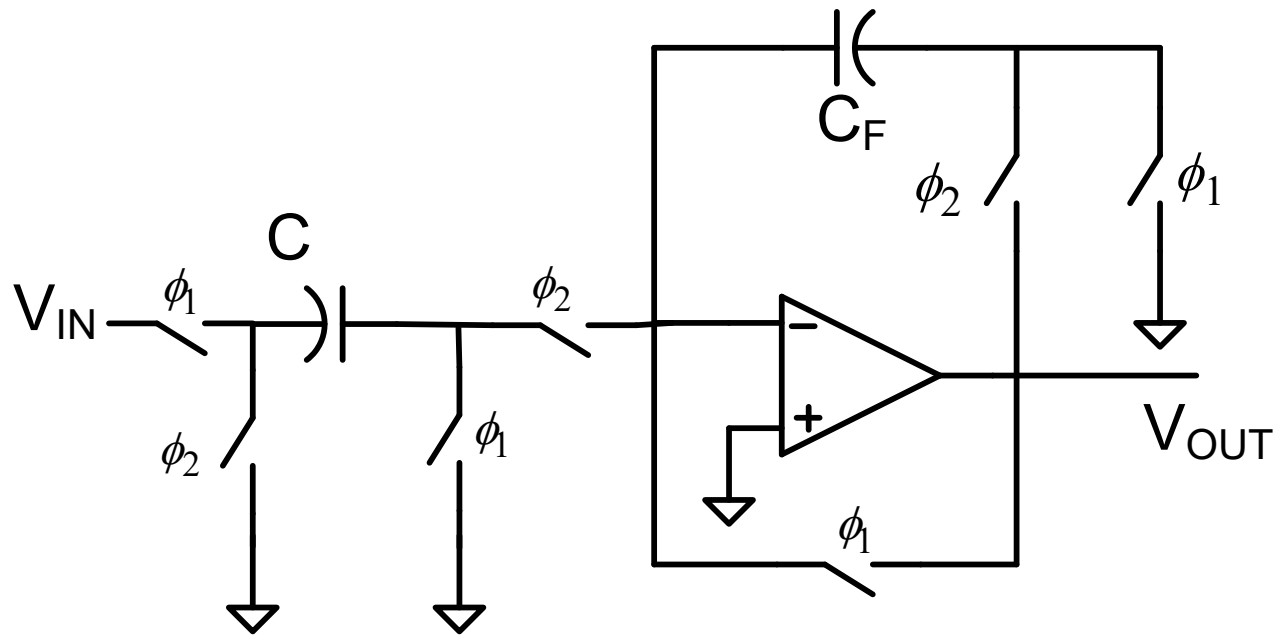
$$\frac{Q_{\phi_1}}{C_F} = V_{OUT}$$

$$\frac{CV_{IN}}{C_F} = V_{OUT}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{C}{C_F}$$

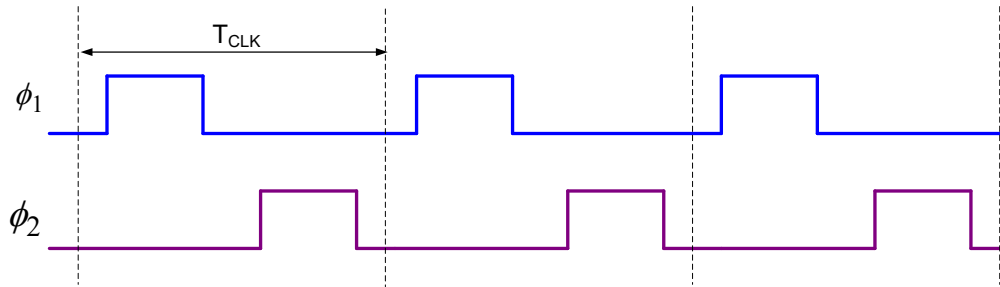
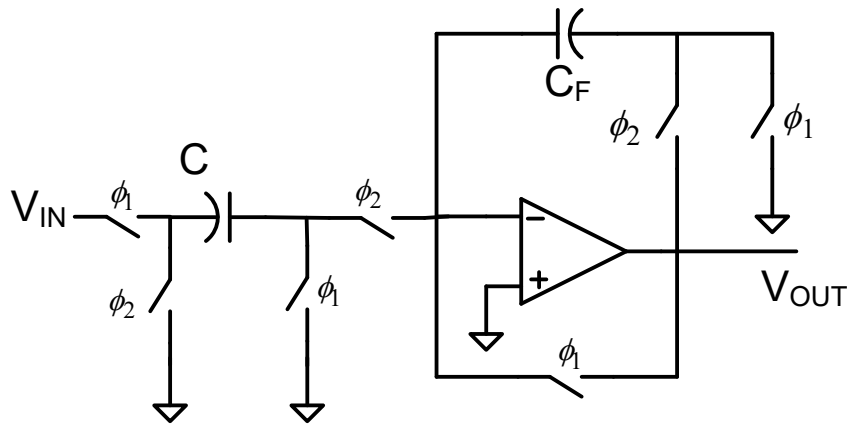
Serves as a noninverting amplifier  
Gain can be very accurate  
Output valid only during  $\Phi_2$

# Another charge redistribution circuit





# A charge redistribution circuit



During phase  $\phi_1$

$$Q_{\phi_1} = CV_{IN}$$

$$Q_{CF} = 0$$

During phase  $\phi_2$

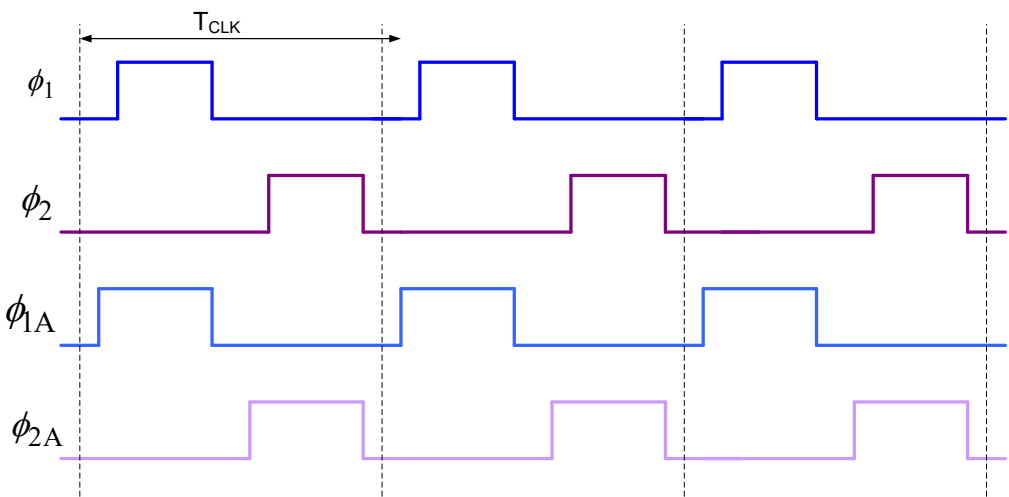
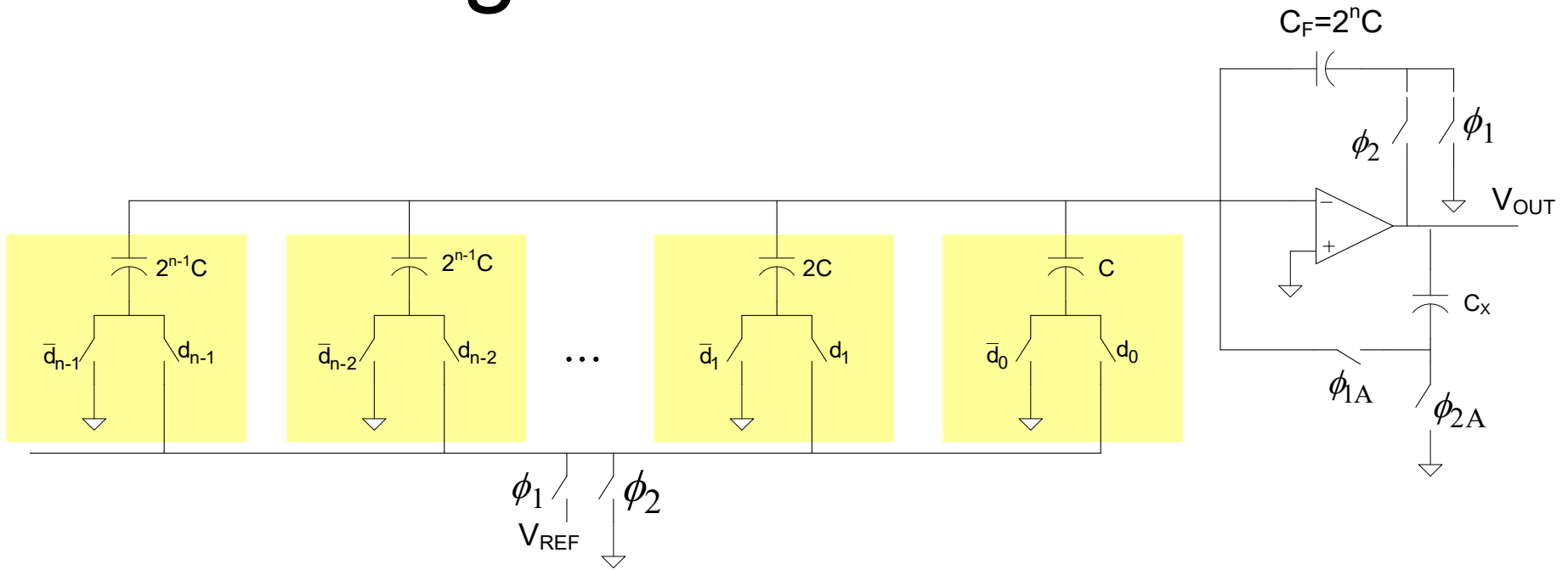
$$\frac{-Q_{\phi_1}}{C_F} = V_{OUT}$$

$$\frac{-CV_{IN}}{C_F} = V_{OUT}$$

$$\frac{V_{OUT}}{V_{IN}} = -\frac{C}{C_F}$$

Serves as an inverting amplifier  
Gain can be very accurate  
Output valid only during  $\Phi_2$

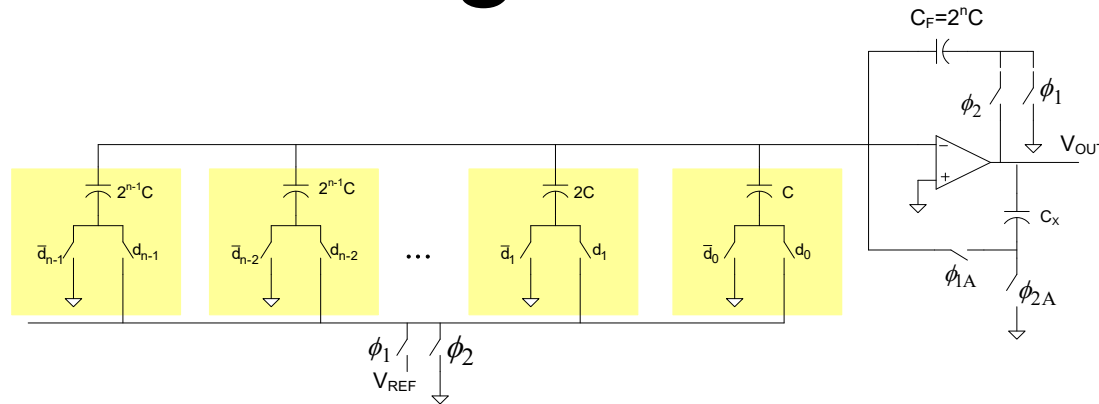
# A charge redistribution DAC



$C_X$  does some good things  
(mitigates  $V_{OS}$ ,  $1/f$  noise and finite gain errors)

Will not consider  $C_X$  affects at this time

# A charge redistribution DAC



**During phase  $\phi_1$**

$$Q_{\phi_1} = V_{REF} \sum_{i=0}^{n-1} d_i \cdot 2^i C$$

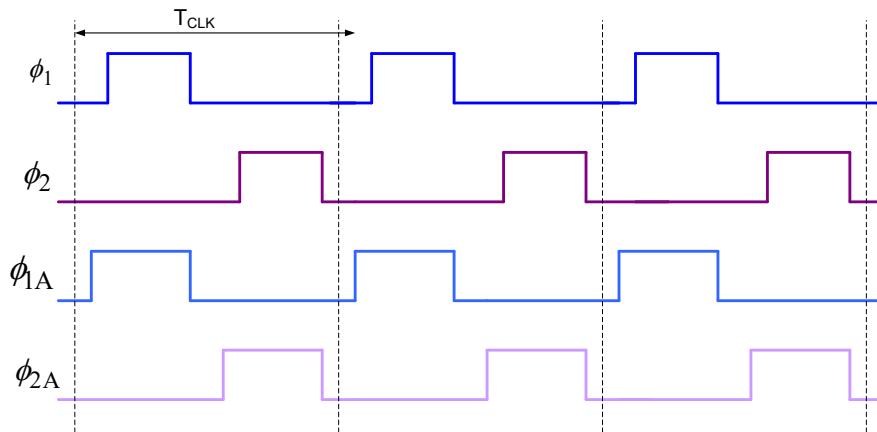
$$Q_{CF} = 0$$

**During phase  $\phi_2$**

$$V_{OUT}(\phi_2) = \frac{1}{C_F} Q_{\phi_1}$$

$$V_{OUT}(\phi_2) = \frac{1}{2^n C} V_{REF} \sum_{i=0}^{n-1} d_i \cdot 2^i C$$

$$V_{OUT}(\phi_2) = V_{REF} \sum_{i=0}^{n-1} \frac{d_i}{2^{n-i}}$$

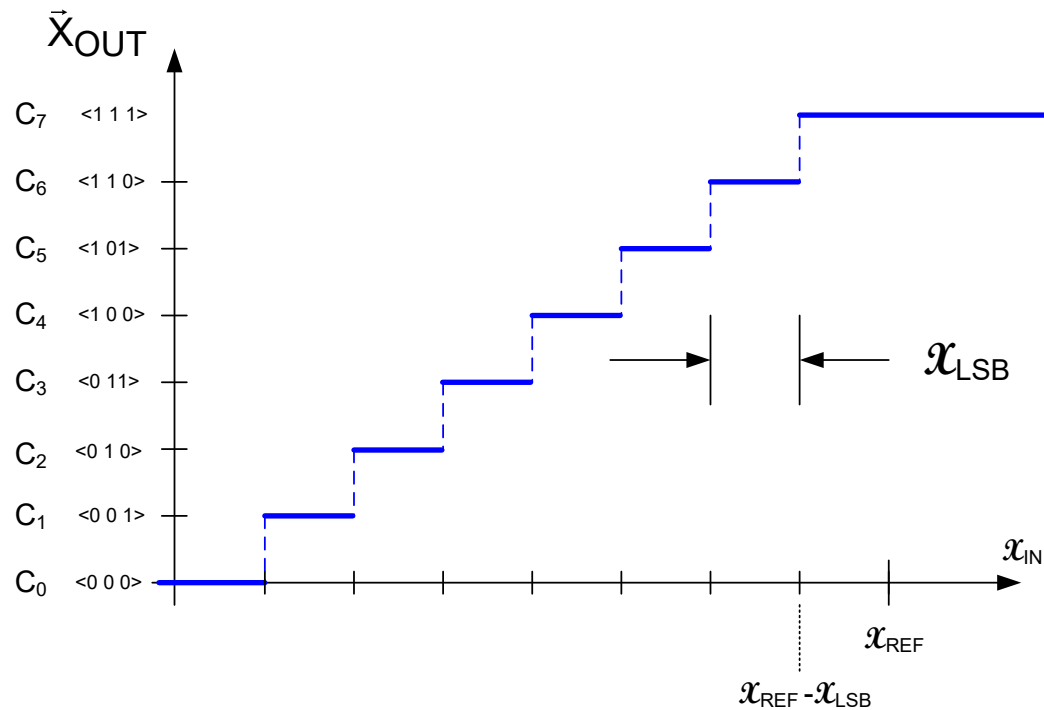


# Analog to Digital Converters



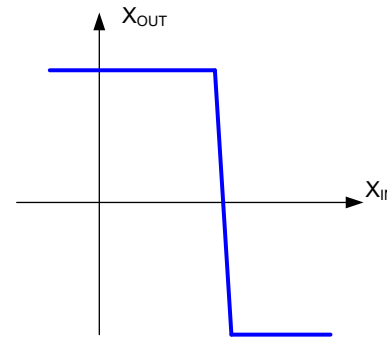
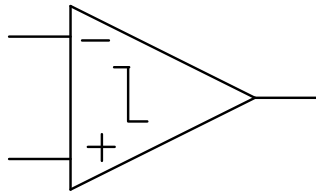
Will now focus on design of ADCs

# Analog to Digital Converters



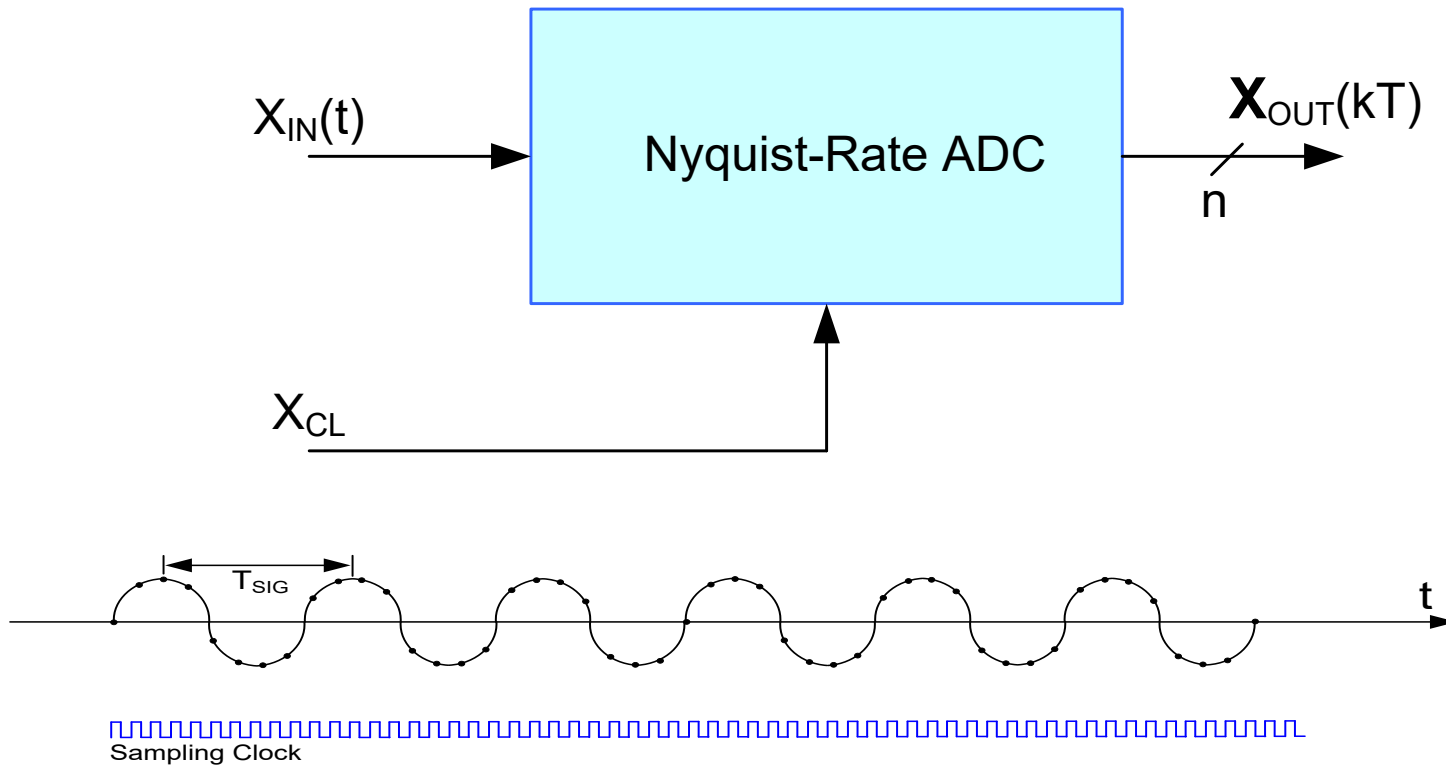
# Analog to Digital Converters

The conversion from analog to digital in most ADCs is done with comparators



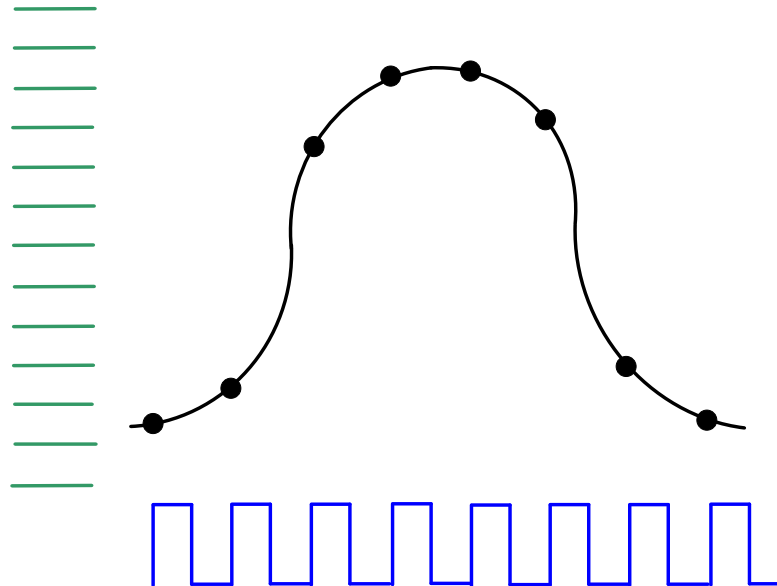
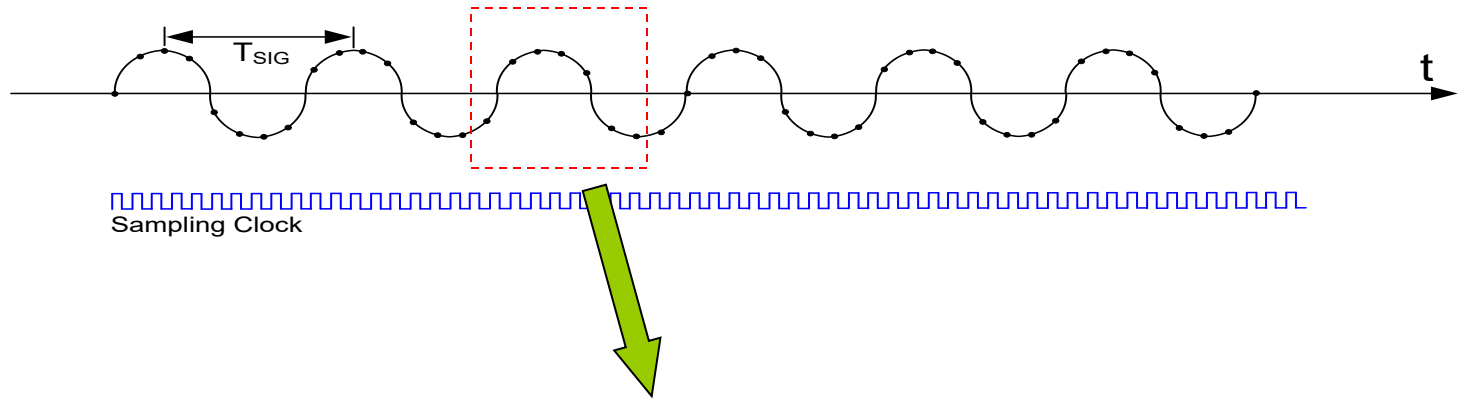
Most ADC design is primarily involved with designing comparators and embedding these into circuits that are robust to nonideal effects

# Nyquist Rate



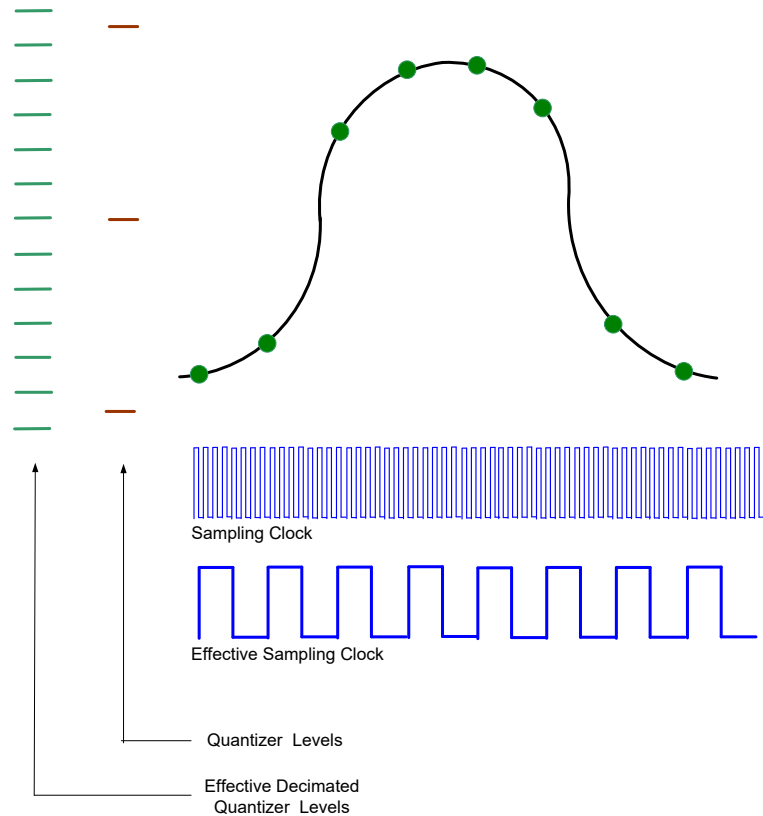
Nyquist Rate Data Converters provide one output for each period of the sampling clock

# Nyquist Rate





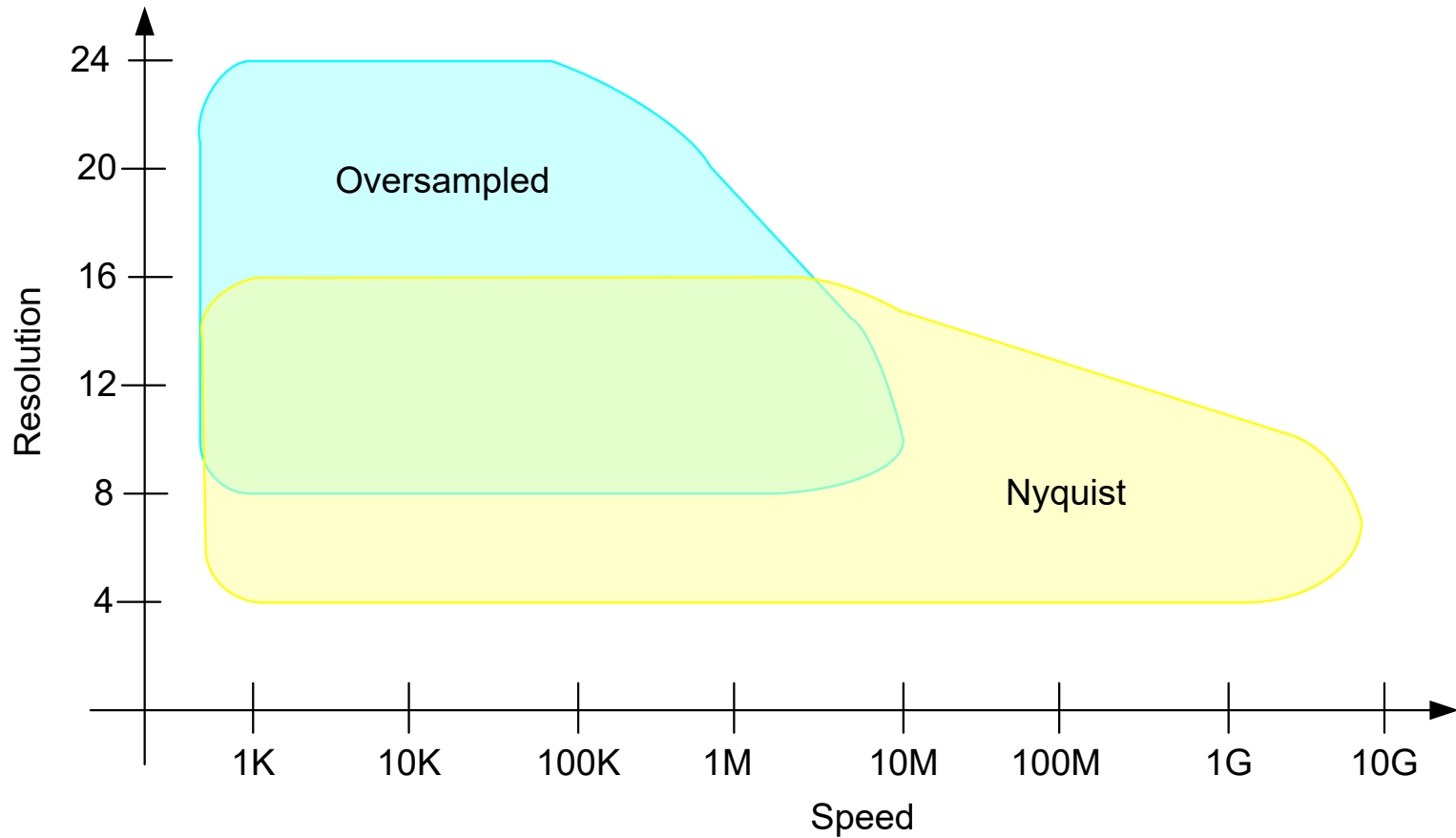
# Over-Sampled



Over-Sampled Data Converters require multiple sampling clock periods for each output

Over-sampling ratios of 128:1 or 64:1 are common  
Dramatic reduction in quantization noise effects  
Limited to relatively low effective conversion rates

# Data Converter Type Chart



# ADC Types

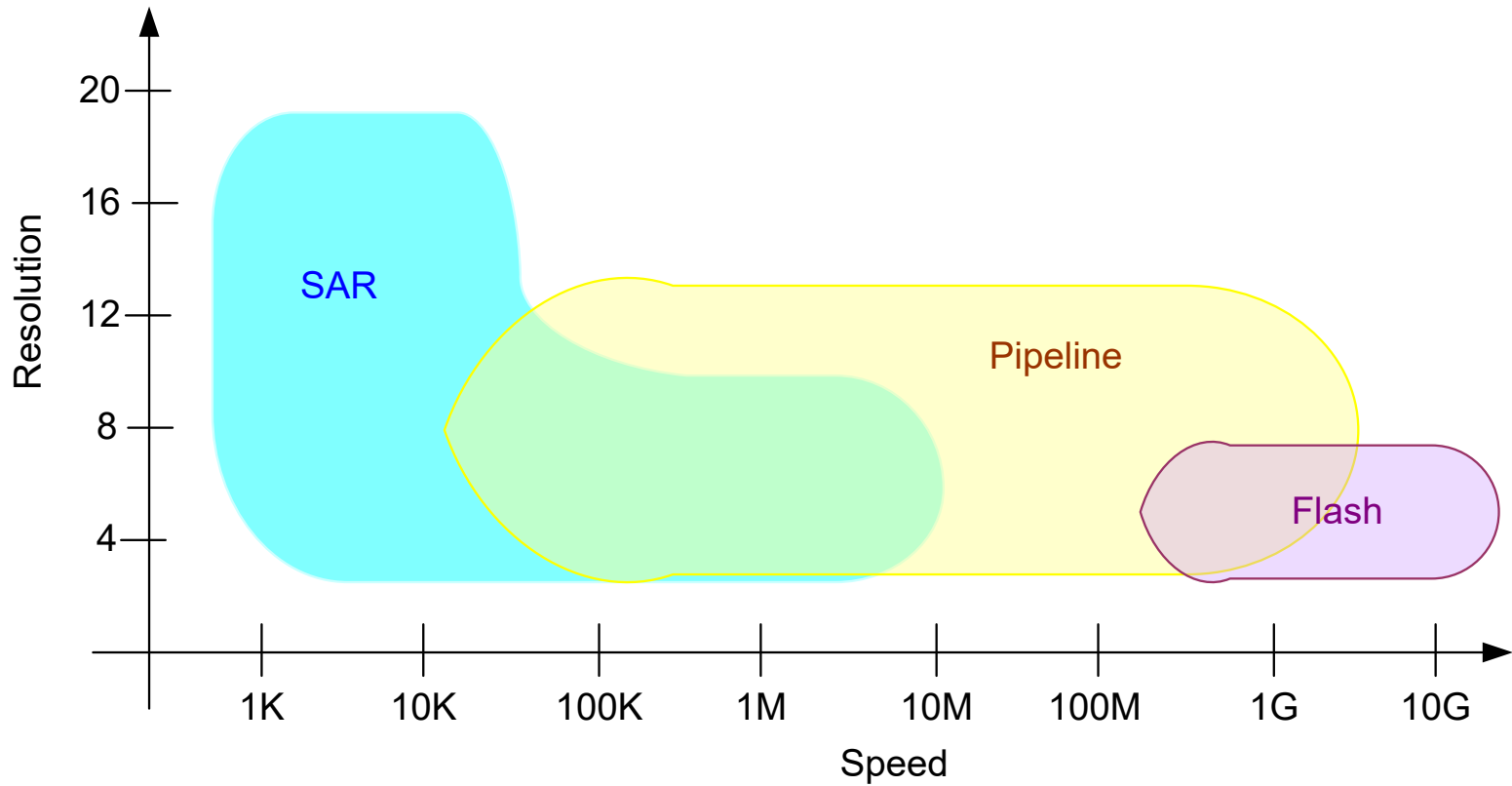
## Nyquist Rate

- Flash
- Pipeline
- Two-Step Flash
- Multi-Step Flash
- Cyclic (algorithmic)
- Interpolating
- Successive Approximation
- Folded
- Dual Slope

## Over-Sampled

- Single-bit
- Multi-bit
- First-order
- Higher-order
- Continuous-time

# Nyquist Rate Usage Structures



# ADC Types

## Nyquist Rate

- Flash
- Pipeline
- Two-Step Flash
- Multi-Step Flash
- Cyclic (algorithmic)
- Interpolating
- Successive Approximation
- Folded
- Dual Slope

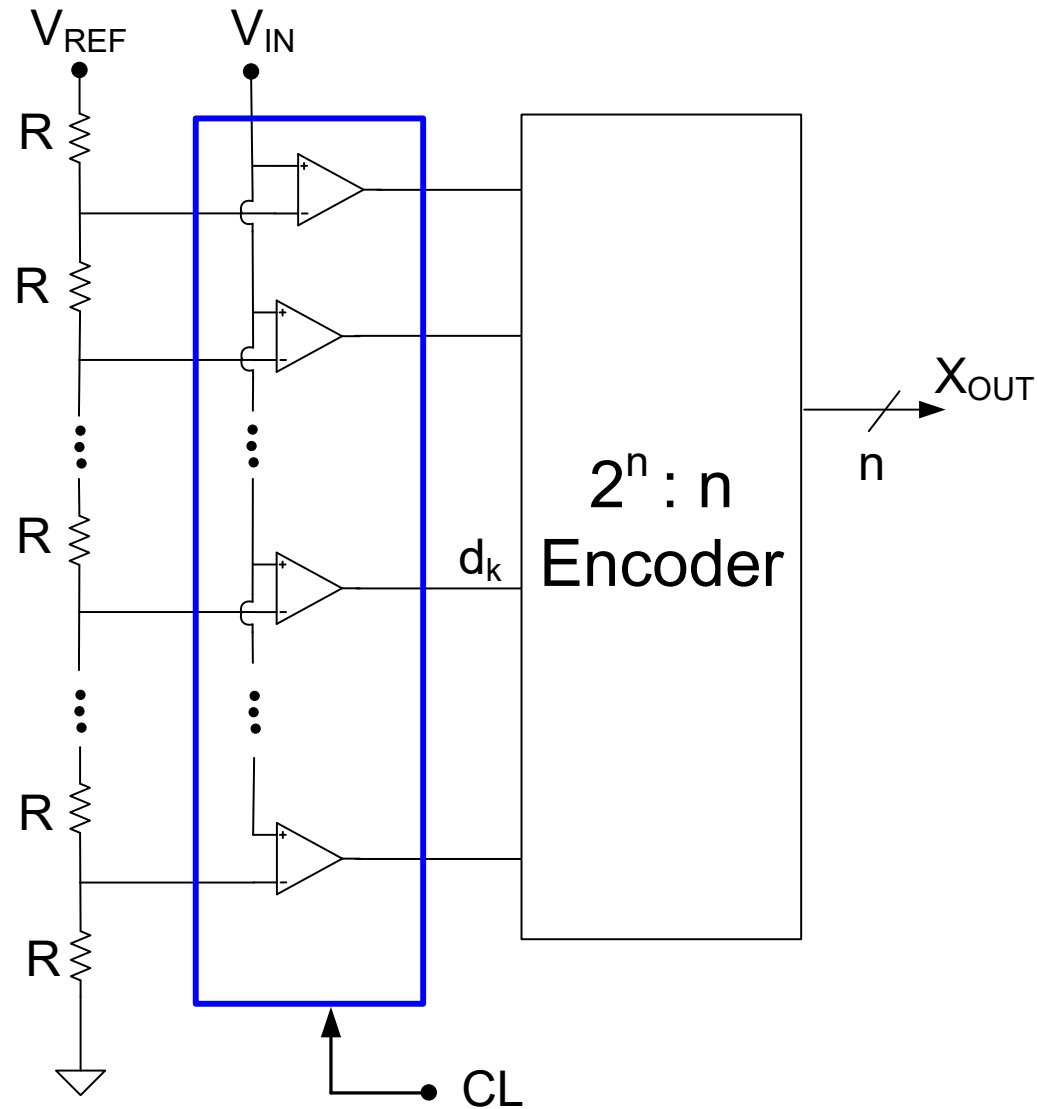
## Over-Sampled

- Single-bit
- Multi-bit
- First-order
- Higher-order
- Continuous-time

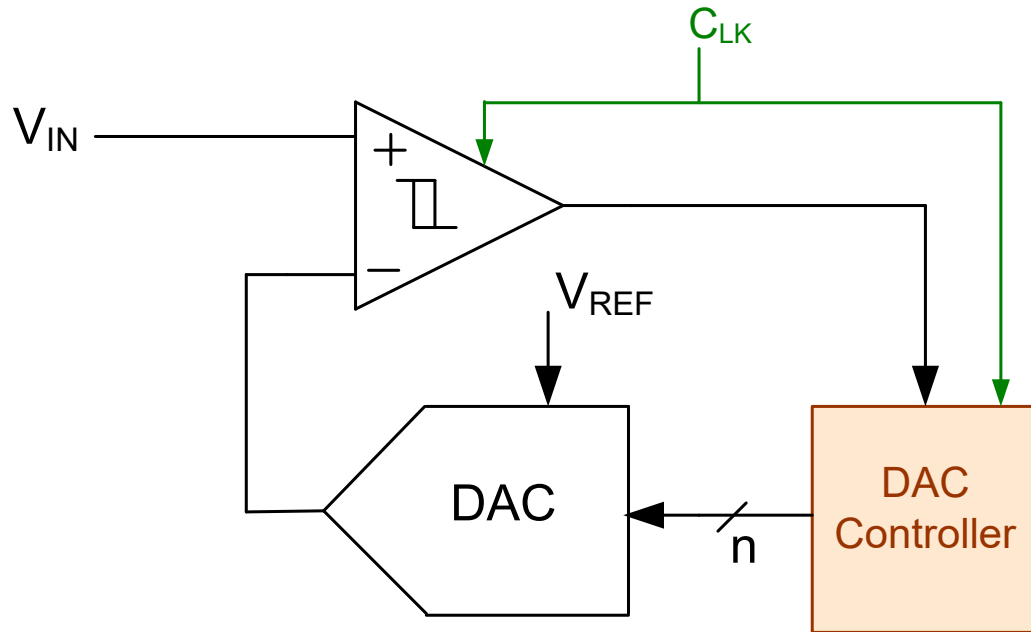
**All have comparable conversion rates**

**Basic approach in all is very similar**

# Flash ADC



# SAR ADC



- DAC Controller may be simply U/D counter
- Binary search controlled by Finite State Machine is faster
- SAR ADC will have no missing codes if DAC is monotone
- Not very fast but can be small



Stay Safe and Stay Healthy !



End of Lecture 35